AMENDMENTS TO THE SPECIFICATION

Please amend the Brief Description of the Drawings section beginning on page 4, line 7 as follows:

Figures 1A and 1B are ~~Figure 1 is~~ a block diagram of circuitry for monitoring the state of two switches;

Figures 2A and 2B are ~~Figure 2 is~~ a schematic of one or more blocks in the diagram of ~~Figure 1~~ Figures 1A and 1B;

Figures 3A and 3B ~~Figure 3 is~~ are a schematic of one or more other blocks in the diagram of ~~Figure 1~~ Figures 1A and 1B;

Figure 4 is a simplified schematic of a portion of the schematic of ~~Figure 3~~ Figures 3A and 3B;

Figures 5 and 6 are schematics of sub-circuits shown in ~~Figure 2~~ Figures 2A and 2B; and

Figure 7 is a flow chart illustrating an operation of the circuitry of ~~Figure 1~~ Figures 1A and 1B.

Please amend the paragraph beginning on page 5, line 10 as follows:

Figures 1A and 1B illustrate ~~Figure 1 illustrates~~ a block diagram of the detection circuitry 1 associated with two switches S1 and S2. Switches S1 and S2 may be of virtually any switch type, and are depicted in symbolic form for reasons of simplicity. Each switch S1 and S2 has a conduction terminal coupled to detection circuitry 1. A conduction terminal of switch S1 is coupled to node TP1 of detection circuitry 1, and a conduction terminal of switch S2 is coupled to node TP2. The configuration register (not shown) may provide many of the input signals to detection circuitry 1.

Please amend the paragraph beginning on page 6, line 7 as follows:

Figures 2A and 2B are ~~Figure 2 is~~ a diagram of a normally open circuit 3. Circuitry 100 in roughly the upper half of ~~Figure 2~~ Figures 2A and 2B is the circuitry for monitoring the switch (S1 or S2) in the normally-open-tamper-to-low configuration, and the circuitry 110 in the lower half of ~~Figure 2~~ Figures 2A and 2B is the circuitry for monitoring the switch in the normally-open-tamper-to-high configuration. Circuitry 120 is control logic for selectively configuring and/or enabling one of circuitry 100 and 110. In this way, the value of output signal TB is only based on the selected one of circuitry 100 and circuitry 110.

2

Please amend the paragraph beginning on page 6, line 14 as follows:

In ~~Figure 2~~ Figures 2A and 2B , the input signal TP is coupled to a conduction terminal of a corresponding switch to be monitored.

Please amend the paragraph beginning on page 8, line 9 as follows:

Circuitry 100 of normally open circuit 3 may further include flip flop circuit 11. Flip flop circuit 11 may be a D-type flip flop circuit (as shown in ~~Fig. 2~~ Fig. 2B), but it is understood that flip flop circuit 11 may be other types of flip flop circuits. A data input of flip flop circuit 11 may be coupled to a logic high level, and a reset input of flip flop circuit 11 may be coupled to enable circuitry. The clock input CK and the inverted clock input CKB may be coupled to the output of circuit 45 via logic NAND gate 8. In particular, flip flop circuit 11 will store a logic high value upon the output OUT of circuit 45 transitioning from a logic high level to a logic low level (i.e., a falling edge of output OUT of circuit 45).

Please amend the paragraph beginning on page 11, line 3 as follows:

The output of circuit 45 changing state also causes transistor 47 to be deactivated and the output of control circuit 46 to deselect circuit 45. Because circuitry 110 is disabled by circuit 120 during this time, flip-flop circuit 11 of circuit 120 remains in the reset state and thus allows output signal TB to follow the output of flip flop circuit 11 of circuit 100. Other circuitry, such as circuitry in output circuits 7 (~~Figure 1~~ Figure 1B) to which output signal TB is coupled as an input may detect output signal TB changing logic state and generate a signal TB that initiates further action.

Please amend the paragraph beginning on page 12, line 3 as follows:

Figures 3A and B are ~~Figure 3 is~~ a schematic diagram for each of the normally closed circuits 5 appearing in ~~Figure 1~~ Figures 1A and 1B. Each normally closed circuit 5 may include a string of series-connected resistors and a plurality of pass gate transistors coupled thereto that may be controlled (i.e., activated or deactivated) for configuring detection circuitry 1 to be one of the normally-closed-tamper-to-high and normally-closed-tamper-to-low configurations. The normally closed circuit 5 receives input signal TP which is coupled to a conduction terminal of the switch being monitored.

Please amend the paragraph beginning on page 12, line 9 as follows:

Figure 4 illustrates a simplified schematic of the resistor-pass gate transistor circuitry normally closed circuit 5 of ~~Figure 3~~ Figures 3A and 3B for configuring the detection circuitry 1 to be in one of the normally-closed-tamper-to-high and normally-closed-tamper-to-low configurations. The simplified schematic of Figure 4 shows a resistor R, which may be formed from a plurality of series-connected resistors; transistor 400 coupled between the high reference voltage Vcc and resistor R; transistor 402 coupled between the low reference voltage Vss and resistor R; transistor 403 coupled between input signal TP and the node coupling transistor 400 to resistor R; and transistor 404 coupled between input signal TP and the node coupling transistor 402 to resistor R. The control terminal of each transistor 400-402 is coupled to control signals.

Please amend the paragraph beginning on page 12, line 18 as follows:

When the detection circuitry 1 is configured in the normally-closed-tamper-to-high configuration, transistors 400 and 404 are activated and transistors 402 and 403 are deactivated. This results in resistor R being coupled to the switch being monitored as a pull-up resistor. When the switch is normally closed, input signal TP is pulled to a voltage corresponding to a logic low state due to the drive strength of the switch being greater than that of the pull-up transistor. Then, when the switch is opened, resistor R pulls input signal TP to a voltage representing a logic high state. Input signal TP being in the logic high state causes circuitry in ~~Figure 1~~ Figures 1A and 1B to drive a corresponding output signal TB1 or TB2 to a logic state to initiate additional tasks.

Please amend the paragraph beginning on page 13, line 6 as follows:

When the tamper detect circuitry is configured in the normally-closed-tamper-to-low configuration, transistors 402 and 403 are activated and transistors 400 and 404 are deactivated. This results in resistor R being coupled to input signal TP (and therefore the switch being monitored) as a pull-down resistor. When the switch is normally closed, input signal TP is pulled to a voltage corresponding to a logic high state. Then, when a tamper event occurs, the switch is opened which results in resistor R pulling input signal TP to a voltage representing a logic low state. Input signal TP being in the logic low state causes circuitry in ~~Figure 1~~ Figures 1A and 1B to drive a corresponding output signal TB1 or TB2 to a logic state to initiate additional tasks.

4

Please amend the paragraph beginning on page 13, line 14 as follows:

With reference again to ~~Figure 3~~ Figures 3A and 3B, resistor R is shown coupled to transistors 400-404. Control circuitry 406, whose inputs may be provided by a configuration register (not shown) or another source, controls the state (activation or deactivation) of transistors 400-404.

Please amend the paragraph beginning on page 13, line 17 as follows:

Because the normally-closed tamper configurations result in a current path existing between the high voltage reference Vcc and the low voltage reference Vss prior to the switch being opened, it may be desired to limit current consumption. Accordingly, the circuit in ~~Figure 1~~ Figures 1A and 1B may include circuitry 9 for periodically or occasionally sampling the state of the switch so that this current path does not continuously exist. The sampling circuitry 9 may, for example, include timing circuitry for periodically or occasionally activating at least one of transistors 400 and 404 (instead of the transistor being continuously activated) when the tamper detect circuitry is configured in the normally-closed-tamper-to-high configuration. This periodic or occasional activation of a transistor 400 or 400 interrupts or breaks the current path between the high reference voltage Vcc and the low reference voltage Vss, thereby reducing current dissipation. Conversely, the sampling circuitry 9 may, for example, include timing circuitry for periodically or occasionally activating at least one of transistors 402 and 403 (instead of the transistor being continuously activated) when the tamper detect circuitry is configured in the normally-closed-tamper-to-low configuration. This periodic or occasional activation of a transistor 402 or 403 interrupts or breaks the current path between the high reference voltage Vcc and the low reference voltage Vss, thereby reducing current dissipation. It is understood that the sampling circuitry may interrupt the current path in other ways.

Please amend the paragraph beginning on page 16, line 4 as follows:

In the event detection circuitry 1 is configured in the normally-open-tamper-to-high state, normally closed circuits 3 are disabled and do not perform the above-described detecting. Transistor 47 (~~Figure 2~~ Figures 2A and 2B) is activated and transistor 48 is deactivated by circuit 120 and signals Control1 and Control2. Activated transistor 47 pulls node TP (and hence the conduction terminal coupled thereto) to a logic high value. When a switch closes, such as due to the occurrence of a tamper event, node TP is pulled to a logic low value. This results in transistor 47 being deactivated and flip flop circuit 11 of circuit 100 clocking a logic high data value, which causes output TB to be in a logic high

5

state, which thereupon causes the output of output circuits 7 to indicate the detection of the switch being closed.

Please amend the paragraph beginning on page 16, line 13 as follows:

In the event detection circuitry 1 is configured in the normally-open-tamper-to-low state, normally closed circuits 3 are disabled and do not perform the above-described detecting. Transistor 48 (Figure 2 Figures 2A and 2B) is activated and transistor 47 is deactivated by circuit 120 and signals Control1 and Control2. Activated transistor 48 pulls node TP (and hence the conduction terminal coupled thereto) to a logic low value. When a switch closes, such as due to the occurrence of a tamper event, node TP is pulled to a logic high value. This results in transistor 48 being deactivated and flip flop circuit 11 of circuit 110 clocking a logic high data value, which causes output TB to be in a logic high state, which thereupon causes the output of output circuits 7 to indicate the detection of the switch being closed.